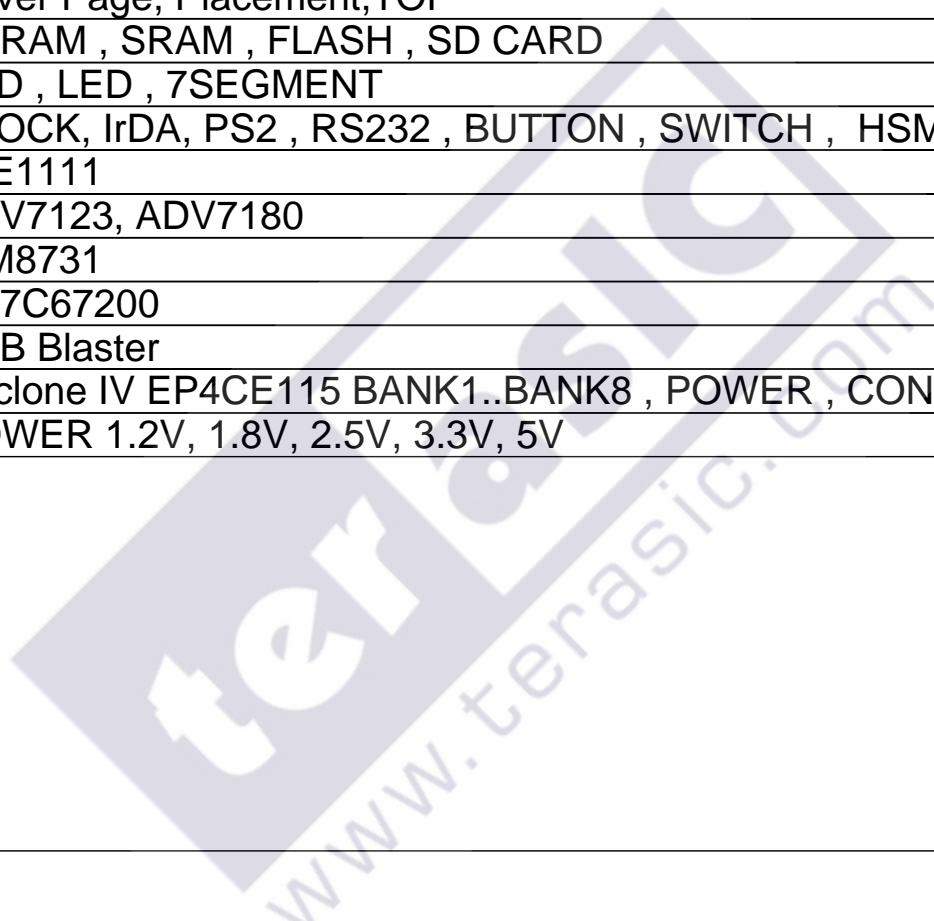
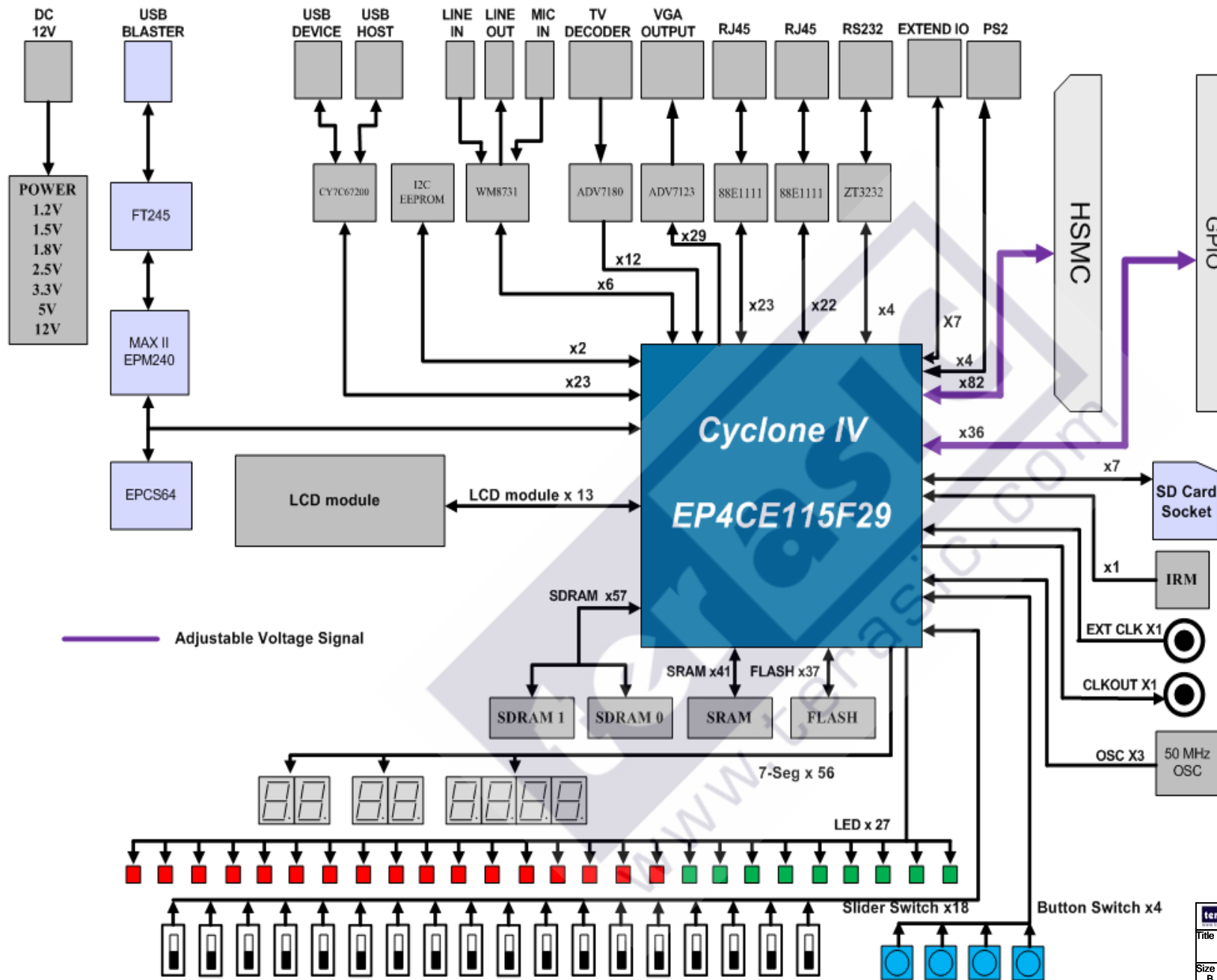





ALTERA Cyclone IV Development & Education Board (DE2-115)

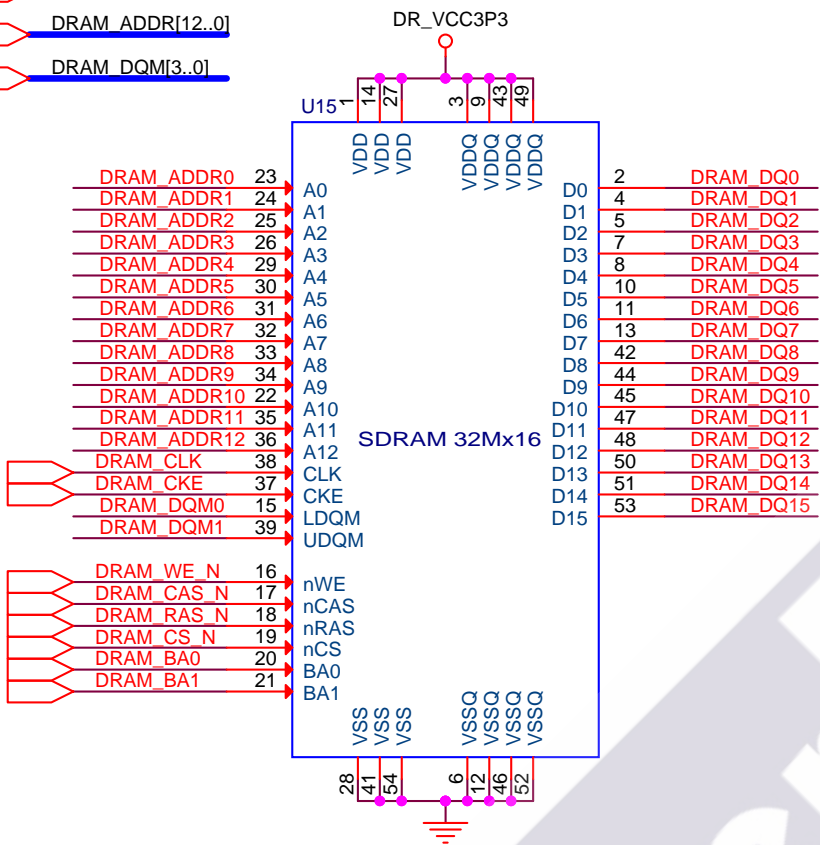
SCHEMATIC	CONTENT	PAGE
01 TOP	Cover Page, Placement, TOP	01 ~ 03
02 MEMORY	SDRAM , SRAM , FLASH , SD CARD	04 ~ 06
03 DISPLAY	LCD , LED , 7SEGMENT	07 ~ 08
04 IN/OUT	CLOCK, IrDA, PS2 , RS232 , BUTTON , SWITCH , HSMC, EEPROM	09 ~ 14
05 ETHERNET	88E1111	15 ~ 16
06 VIDEO	ADV7123, ADV7180	17 ~ 18
07 AUDIO	WM8731	19
08 USB DEVICE	CY7C67200	20
09 FPGA Configuration	USB Blaster	21
10 FPGA	Cyclone IV EP4CE115 BANK1..BANK8 , POWER , CONFIG	22 ~ 26
11 POWER	POWER 1.2V, 1.8V, 2.5V, 3.3V, 5V	27 ~ 28



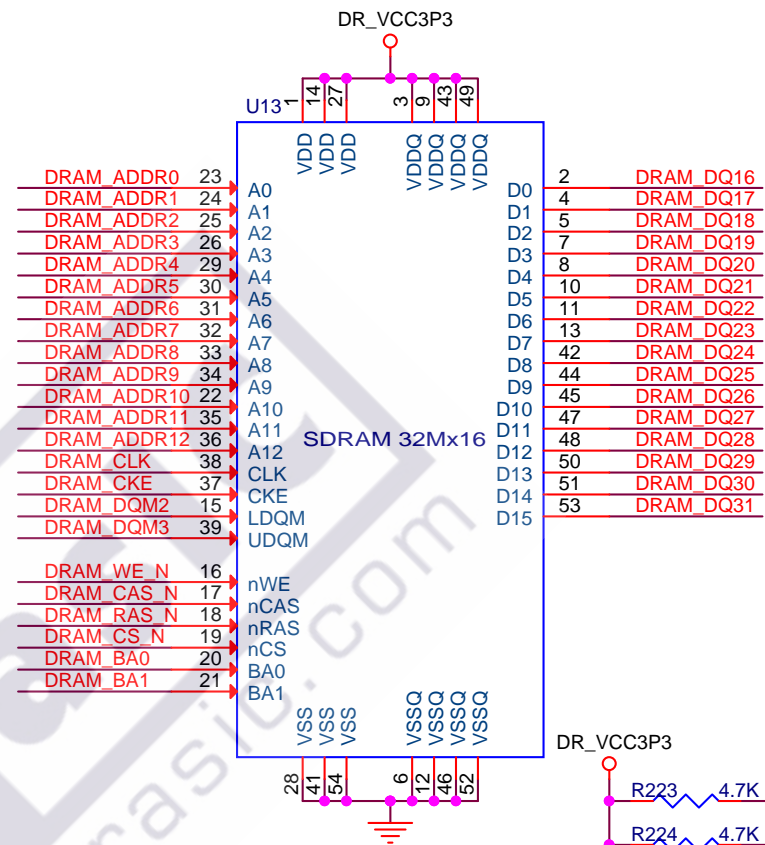


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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	PLACEMENT	D
Date:	Tuesday, April 16, 2013	Sheet 2 of 28

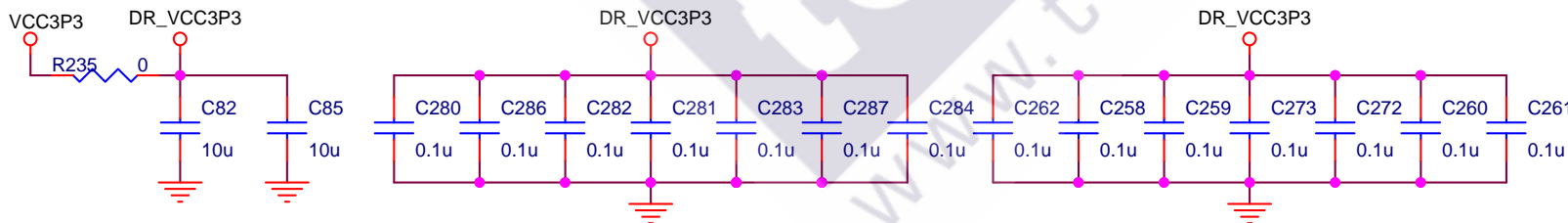
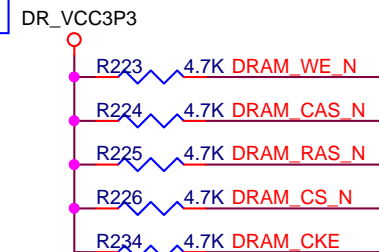
 DRAM DQ[31..0]
 DRAM ADDR[12..0]
 DRAM DQM[3..0]




SDRAM0



SDRAM1

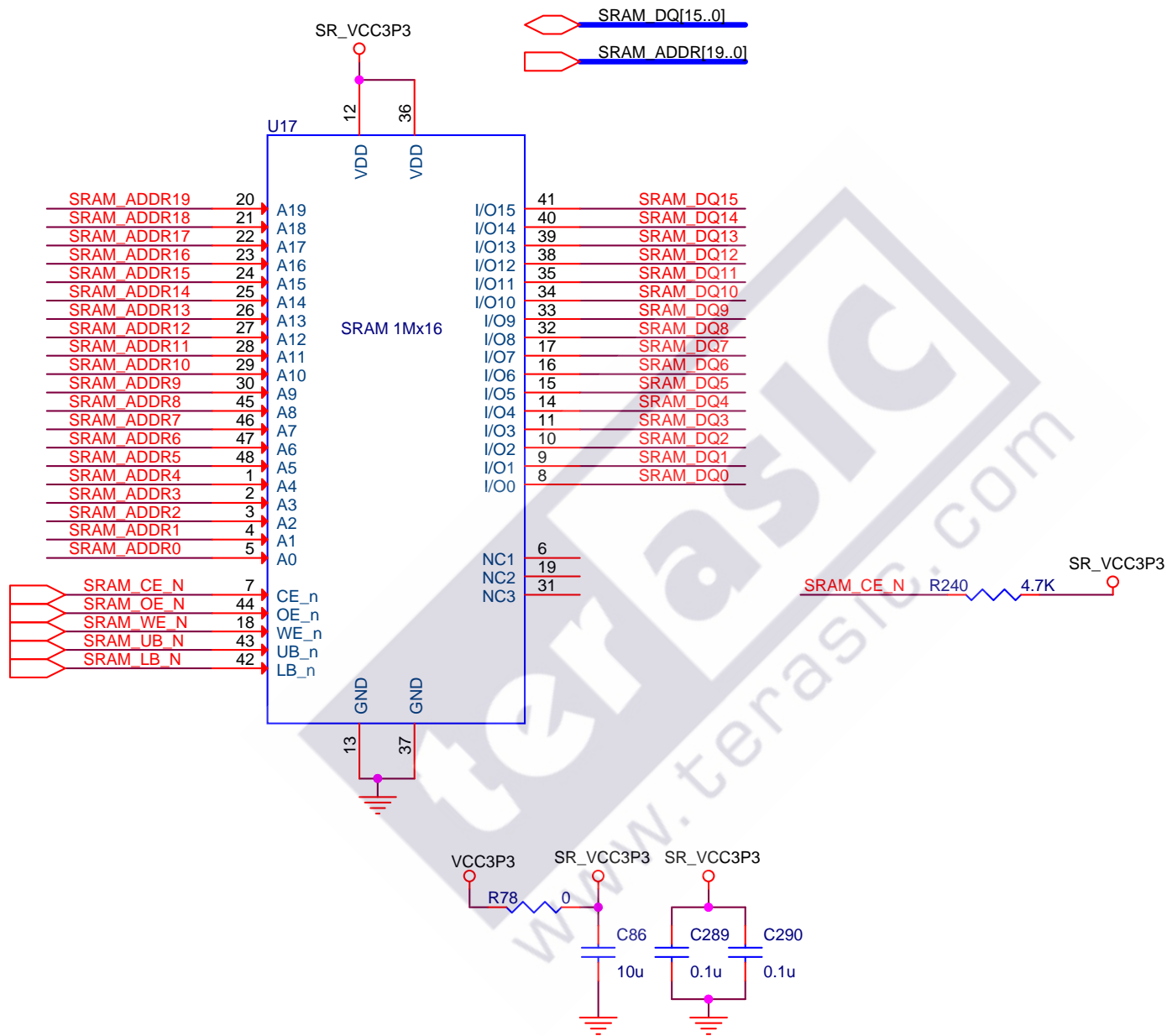



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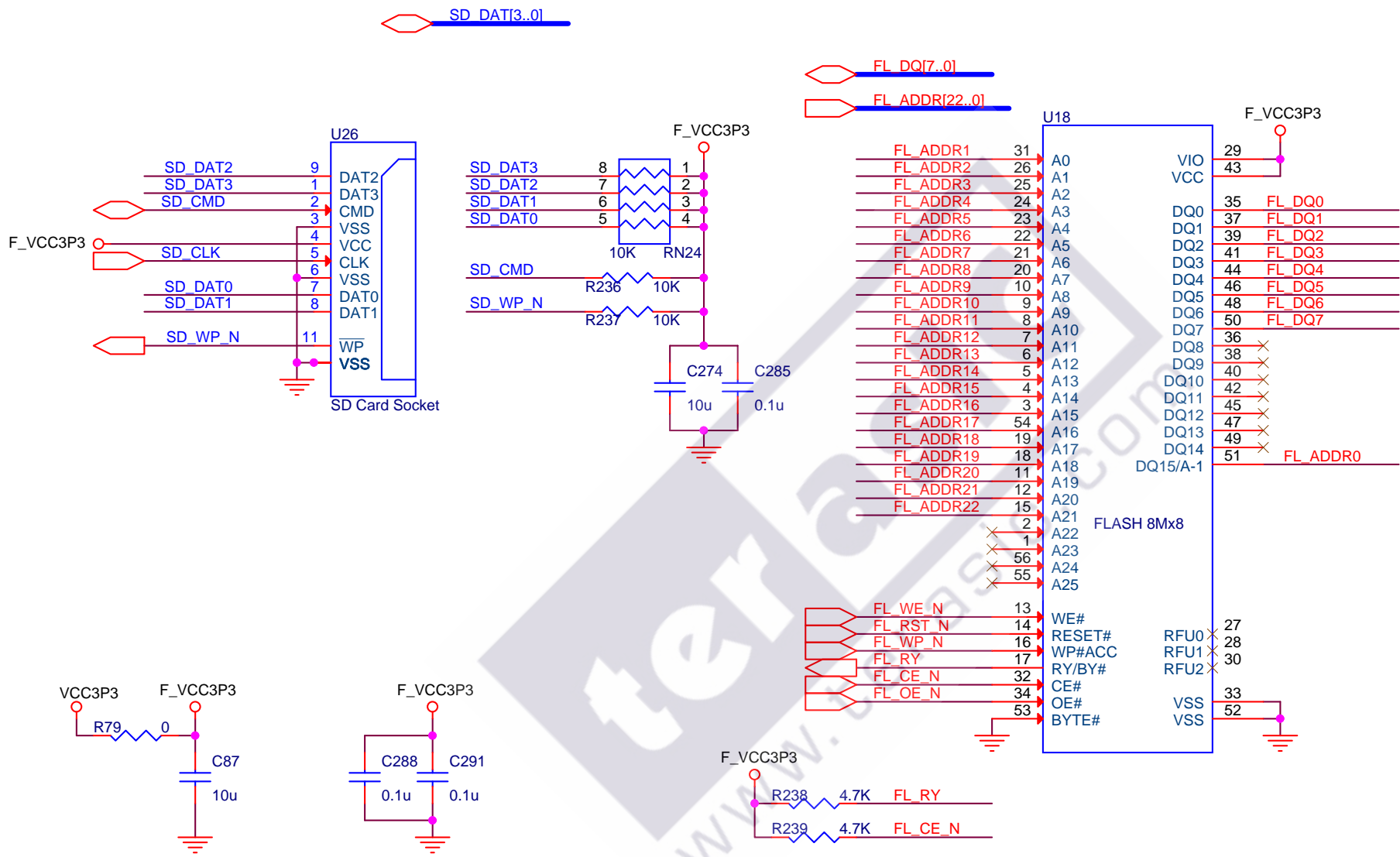
Title
DE2-115 Main Board


Size A	Document Number SDRAM	Rev D
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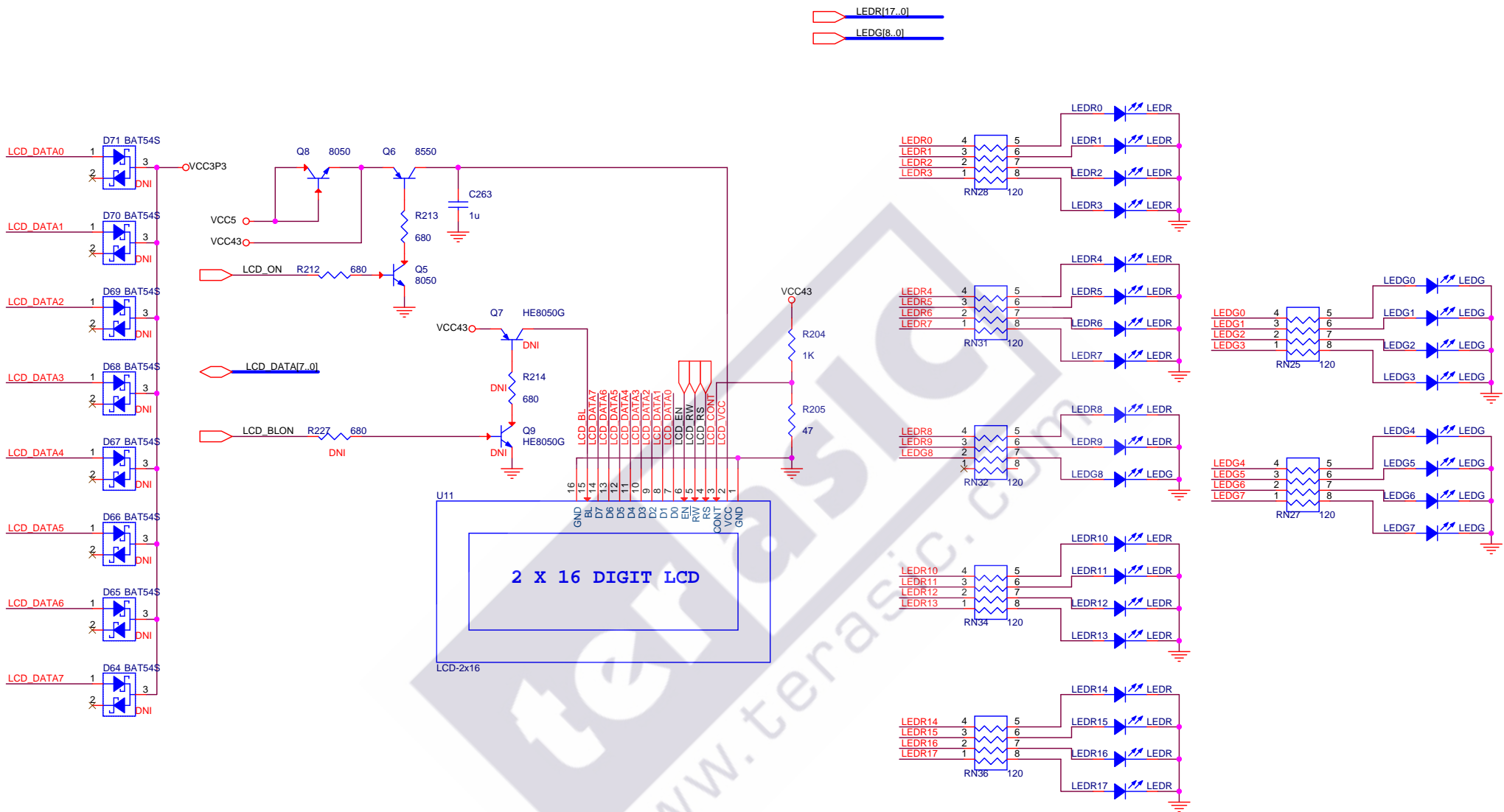
Date: Tuesday, April 16, 2013 **Sheet** 4 **of** 28



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Title		
DE2-115 Main Board		
Size	Document Number	Rev
A	SRAM	D
Date:	Tuesday, April 16, 2013	Sheet 5 of 28



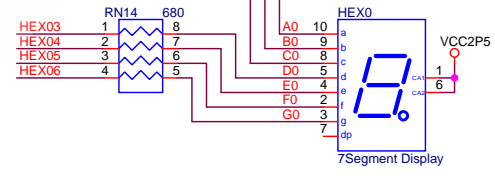
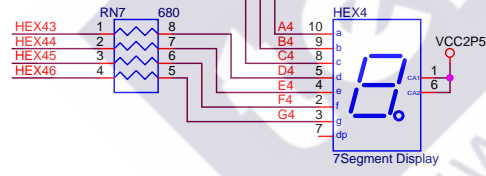
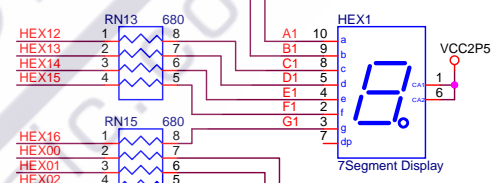
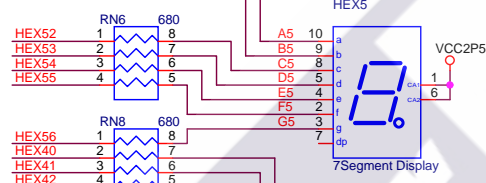
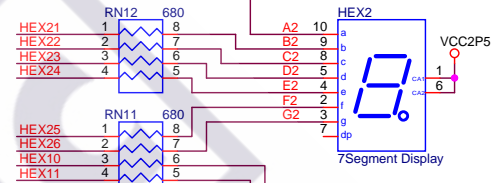
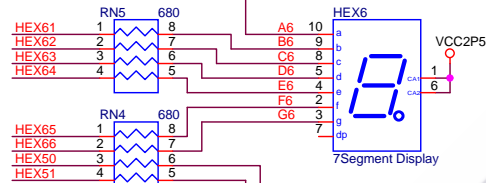
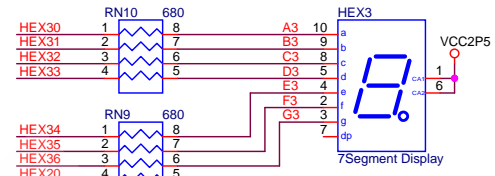
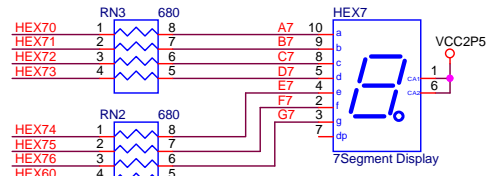
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
A	Flash & SD	D
Date:	Tuesday, April 16, 2013	Sheet 6 of 28



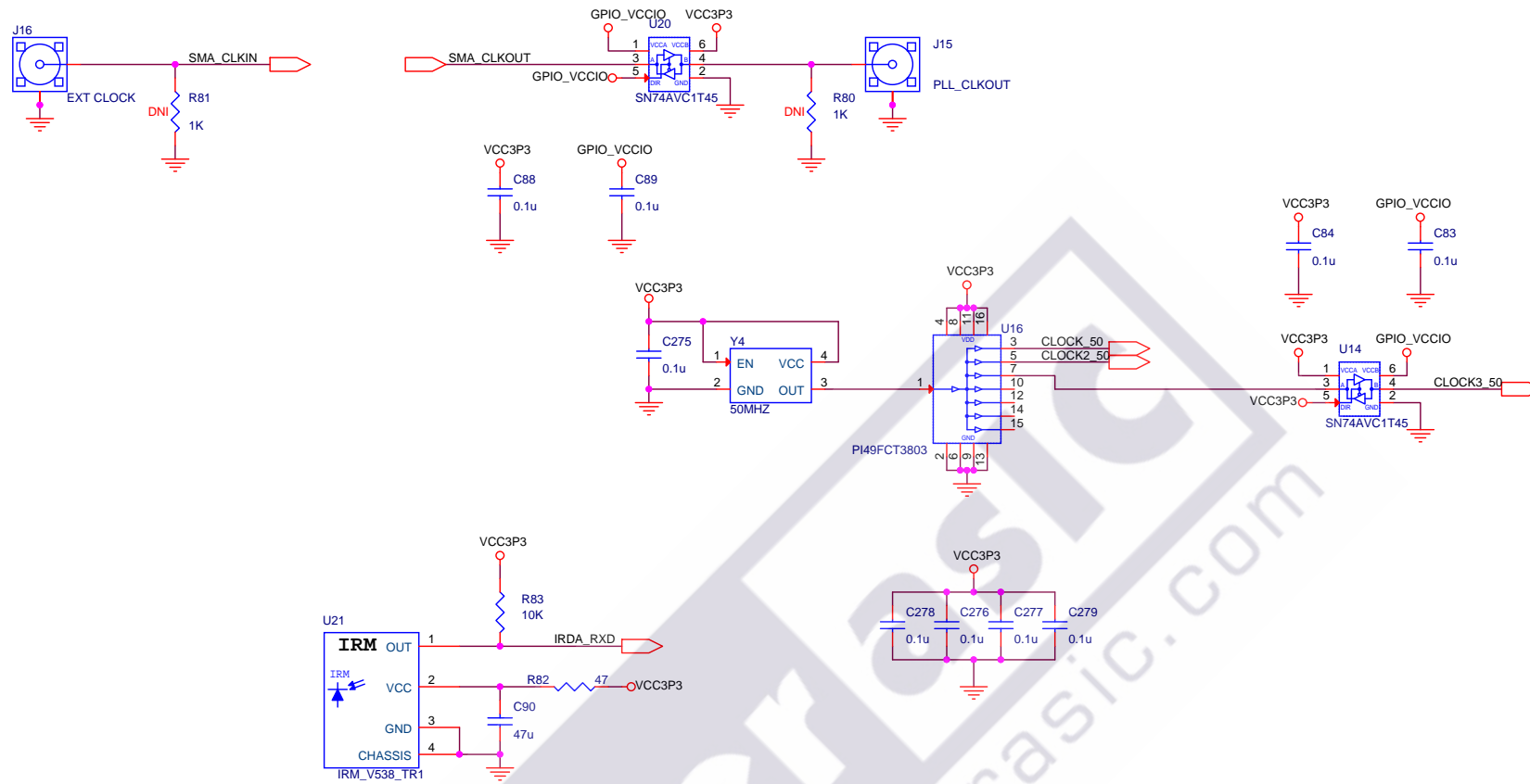
LED R(17..0)
LED G(8..0)


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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	LCD & LED	D
Date:	Tuesday, April 16, 2013	Sheet 7 of 28

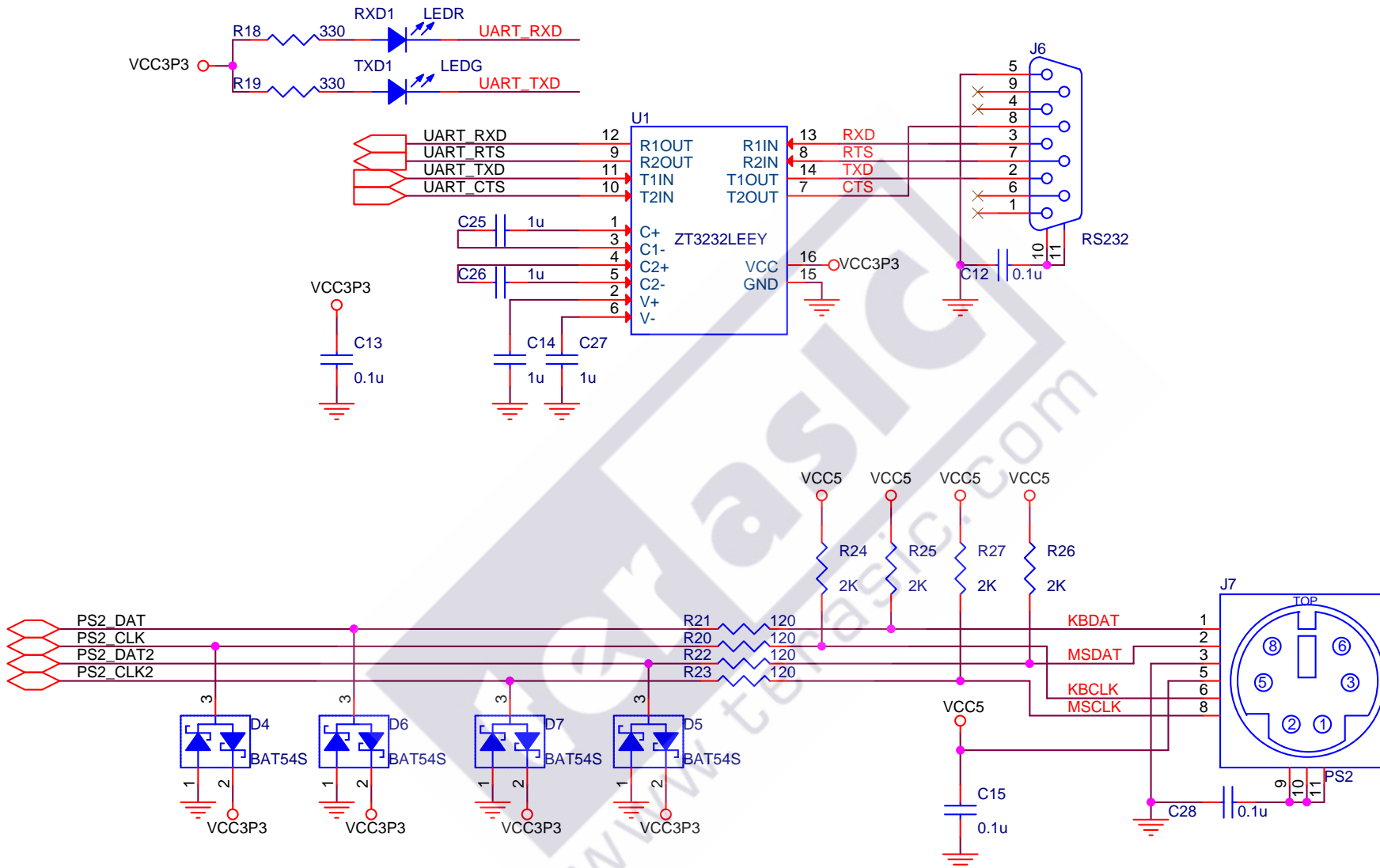
- ▶ HEX0[6..0]
- ▶ HEX1[6..0]
- ▶ HEX2[6..0]
- ▶ HEX3[6..0]
- ▶ HEX4[6..0]
- ▶ HEX5[6..0]
- ▶ HEX6[6..0]
- ▶ HEX7[6..0]




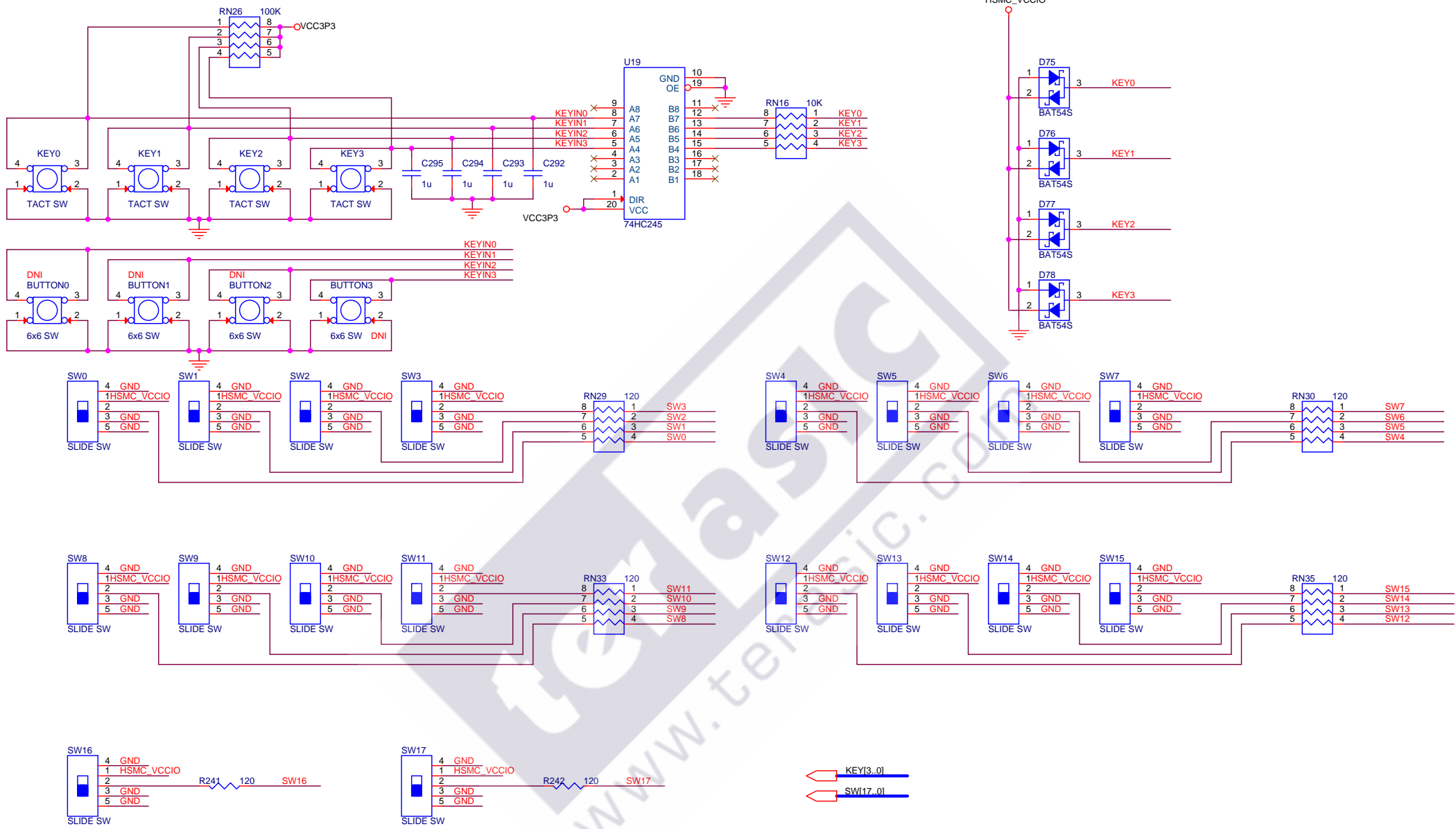
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	LCD & LED	D
Date:	Tuesday, April 16, 2013	Sheet 8 of 28



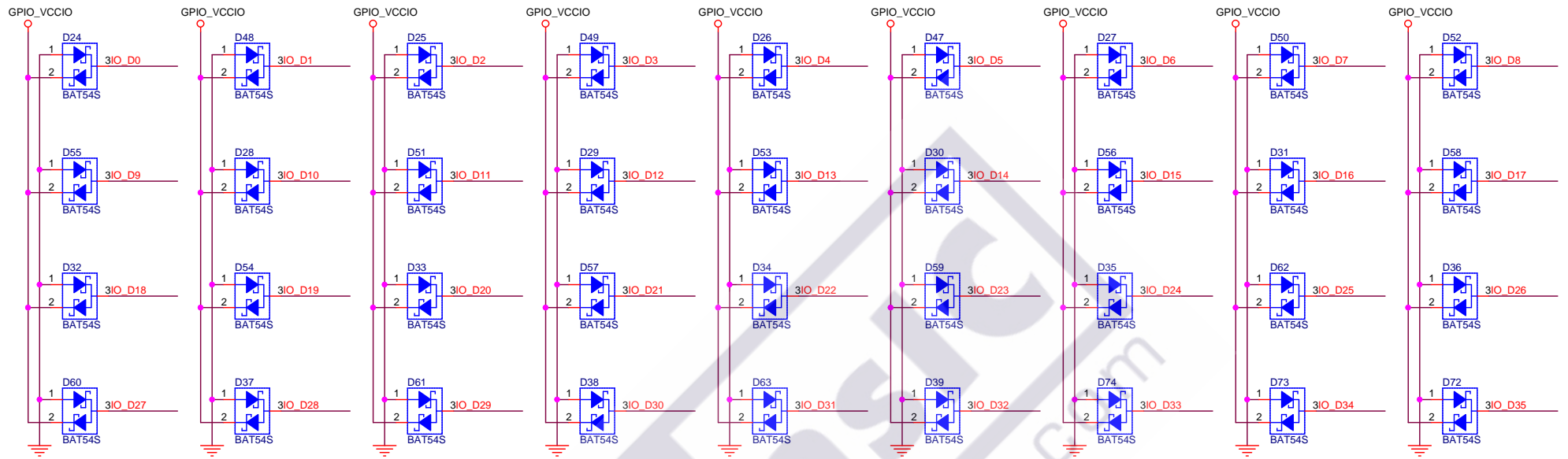
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	CLOCK & IrDA	D
Date:	Tuesday, April 16, 2013	Sheet 9 of 28



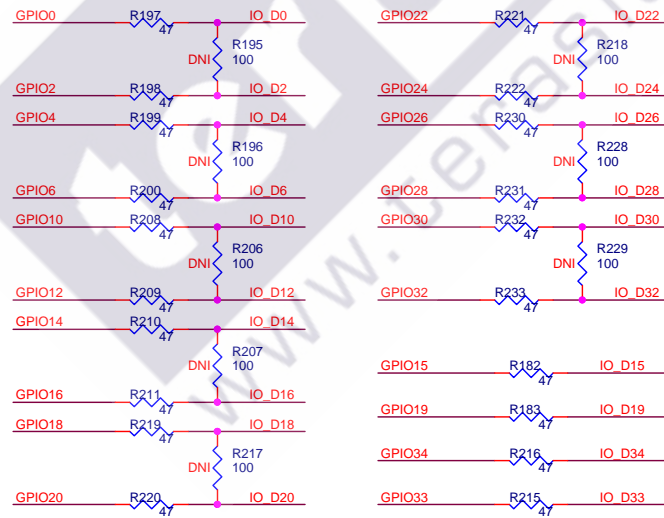
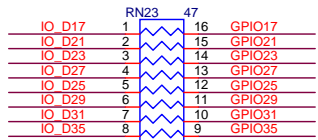
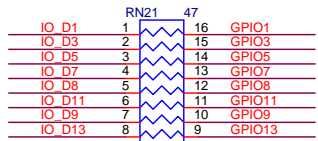
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
A	PS2 & RS232	D
Date:	Tuesday, April 16, 2013	Sheet 10 of 28



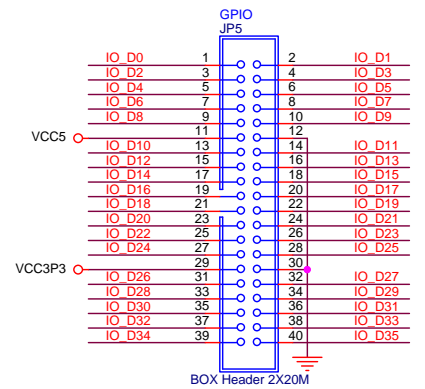
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	BUTTON & SWITCH	D
Date:	Tuesday, April 16, 2013	Sheet 11 of 28



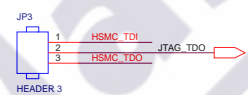
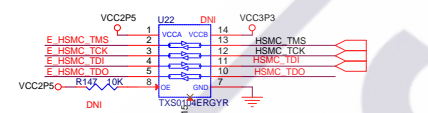
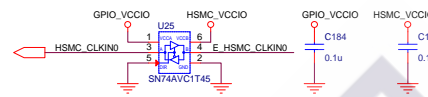
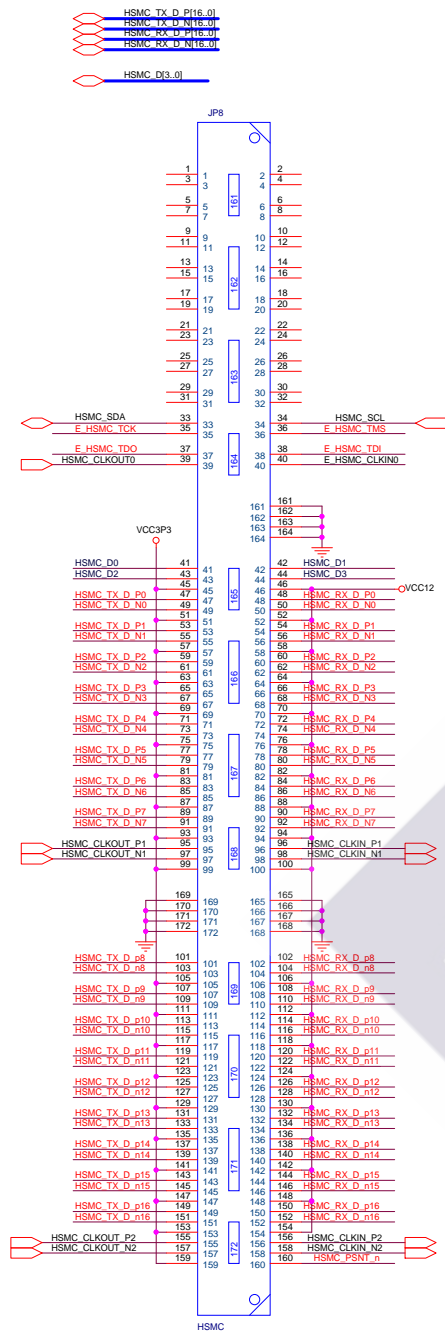
GPIO[35..0]



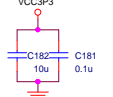
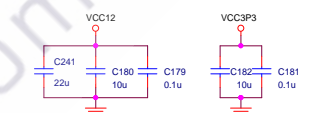
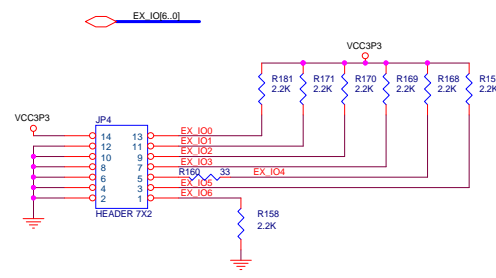
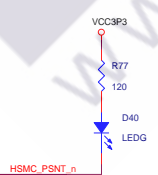
Close to FPGA

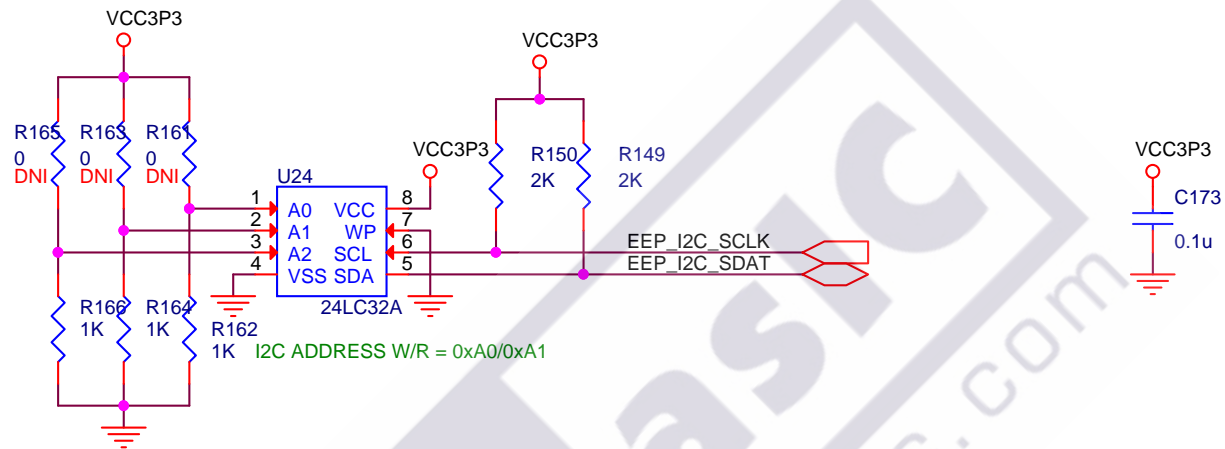


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Title	
DE2-115 Main Board	
Size	Document Number
B	GPIO
Date:	Tuesday, April 16, 2013
Sheet	12 of 28
Rev	D



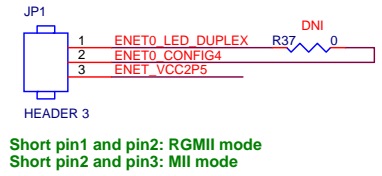
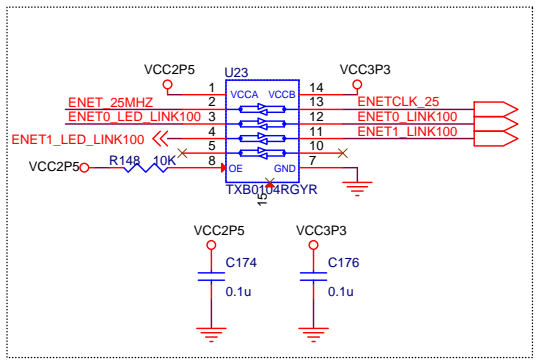
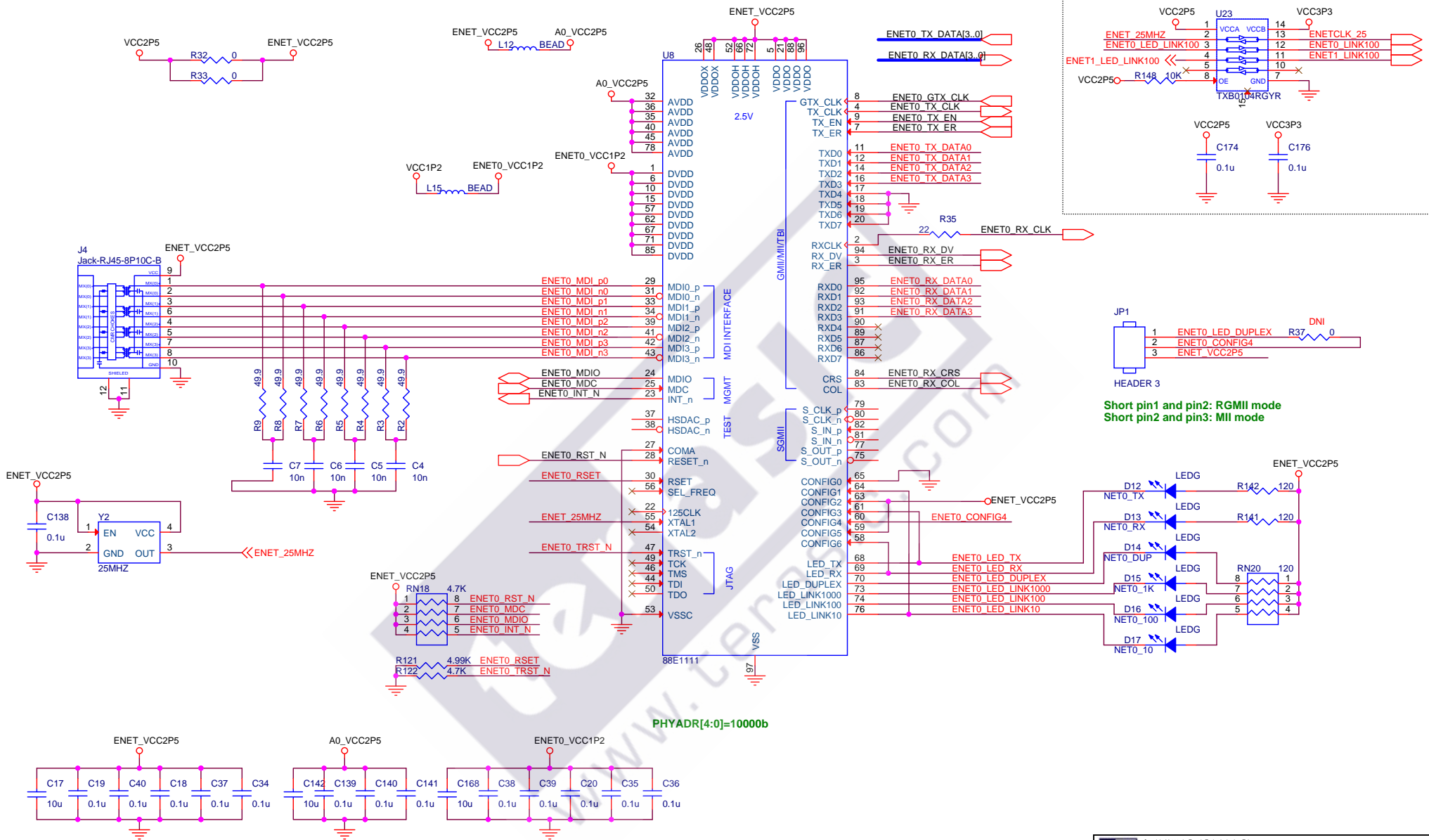
Short pin1 and pin2: JTAG chain not including HSMC
 Short pin2 and pin3: JTAG chain including HSMC





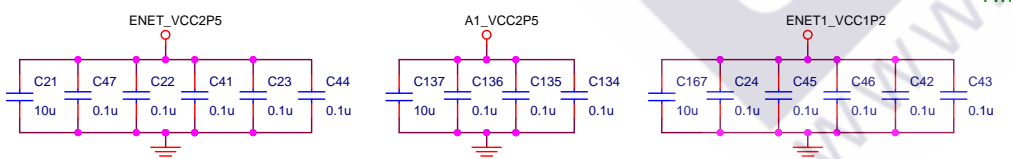
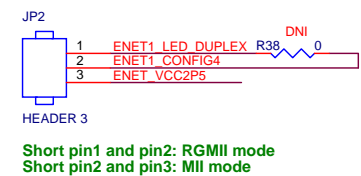
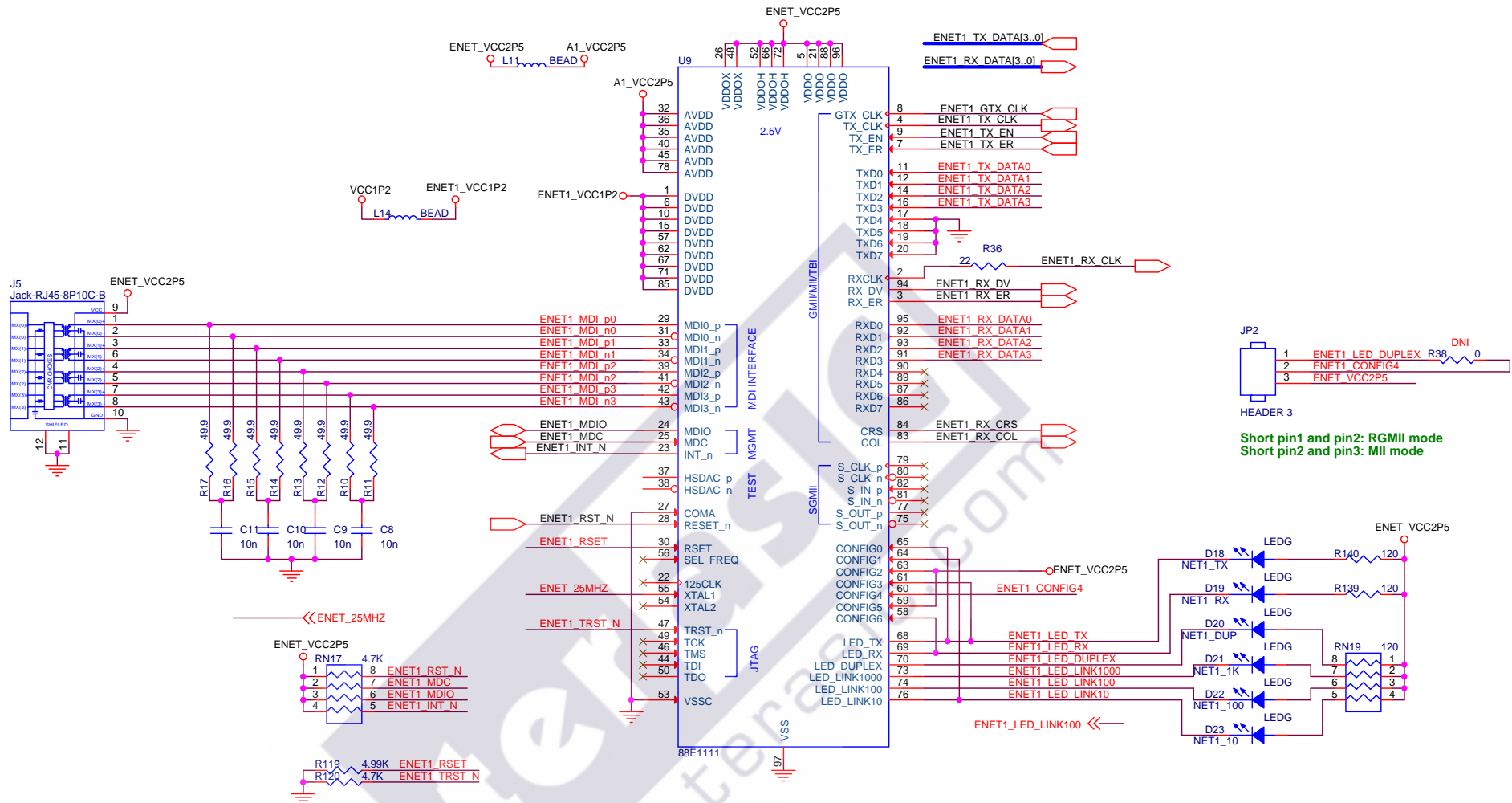
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
A	EEPROM	D
Date:	Tuesday, April 16, 2013	Sheet 14 of 28

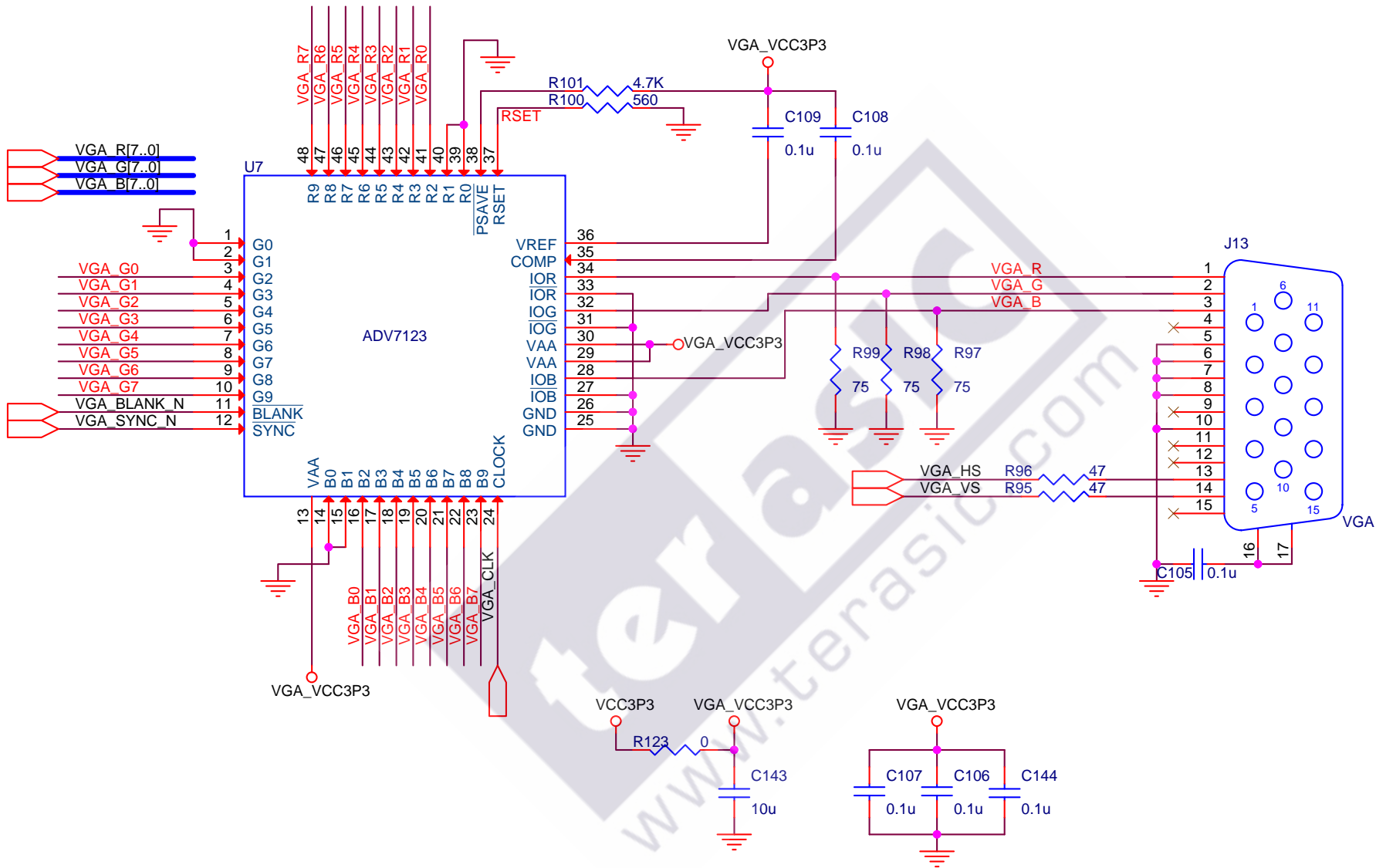



PHYADR[4:0]=10000b

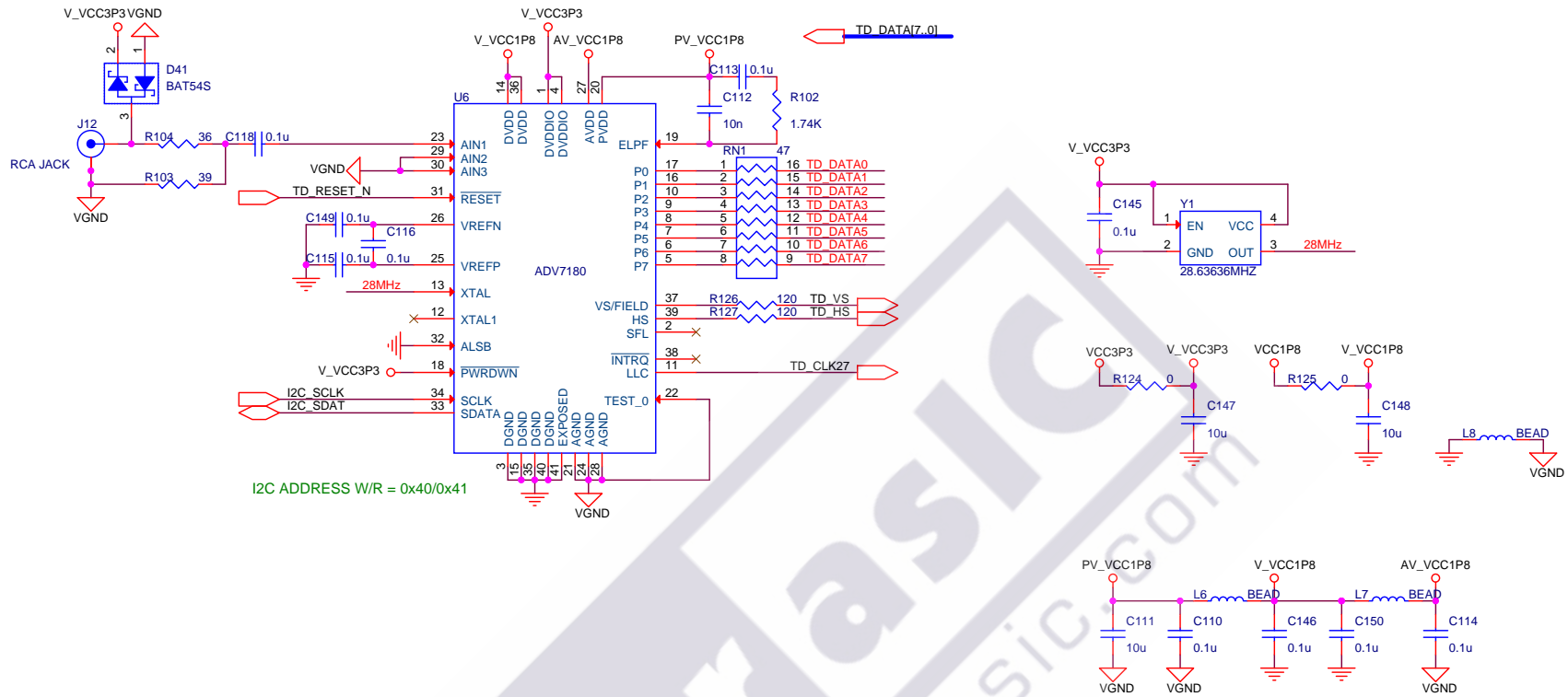
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	Ethernet 0	D
Date:	Tuesday, April 16, 2013	Sheet 15 of 28




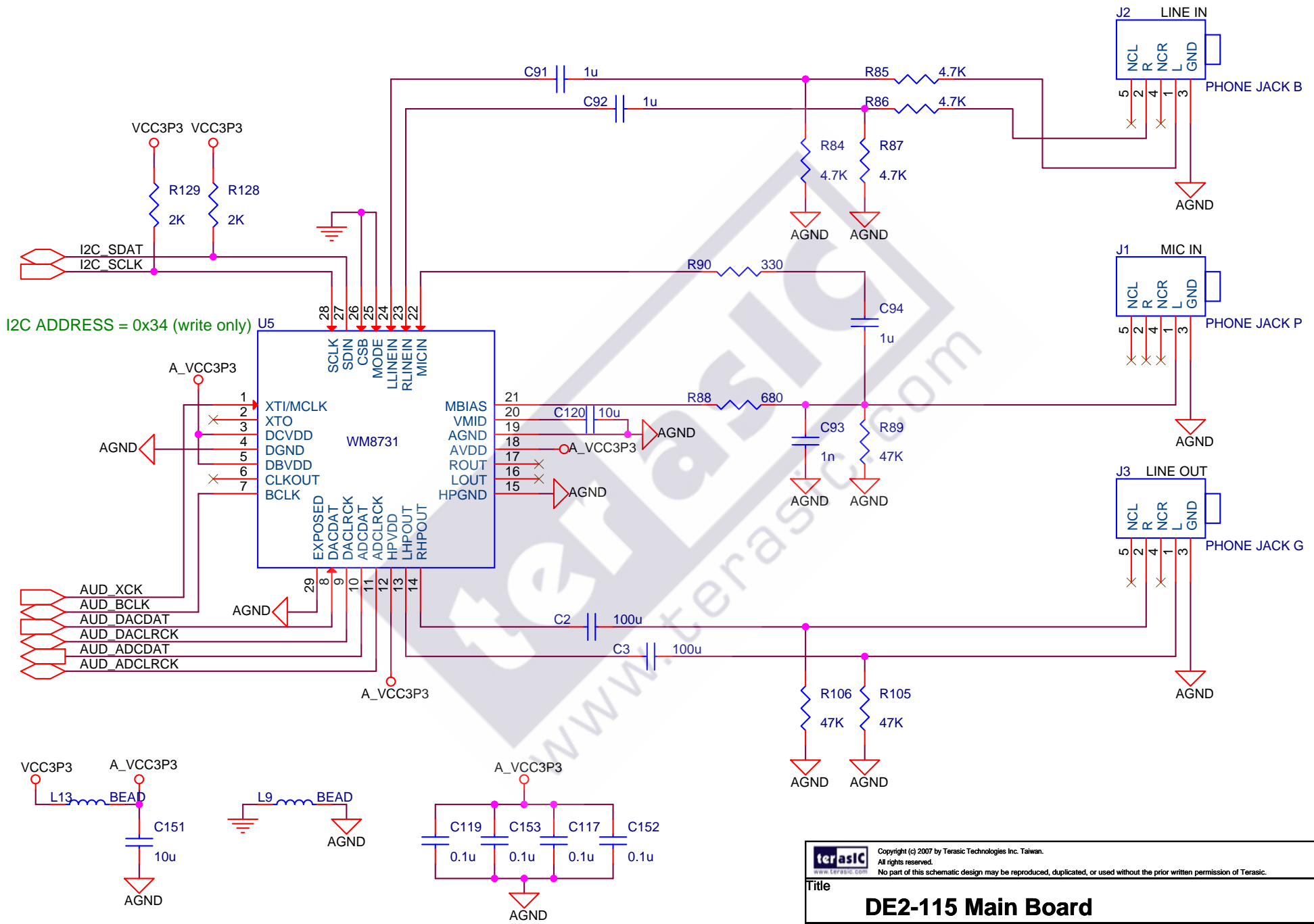
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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	Ethernet 1	D
Date:	Tuesday, April 16, 2013	Sheet 16 of 28




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Title		
DE2-115 Main Board		
Size	Document Number	Rev
A	ADV7123 VGA	D
Date:	Tuesday, April 16, 2013	Sheet 17 of 28



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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	ADV7180 DECODER	D
Date:	Tuesday, April 16, 2013	Sheet 18 of 28



I2C ADDRESS = 0x34 (write only)

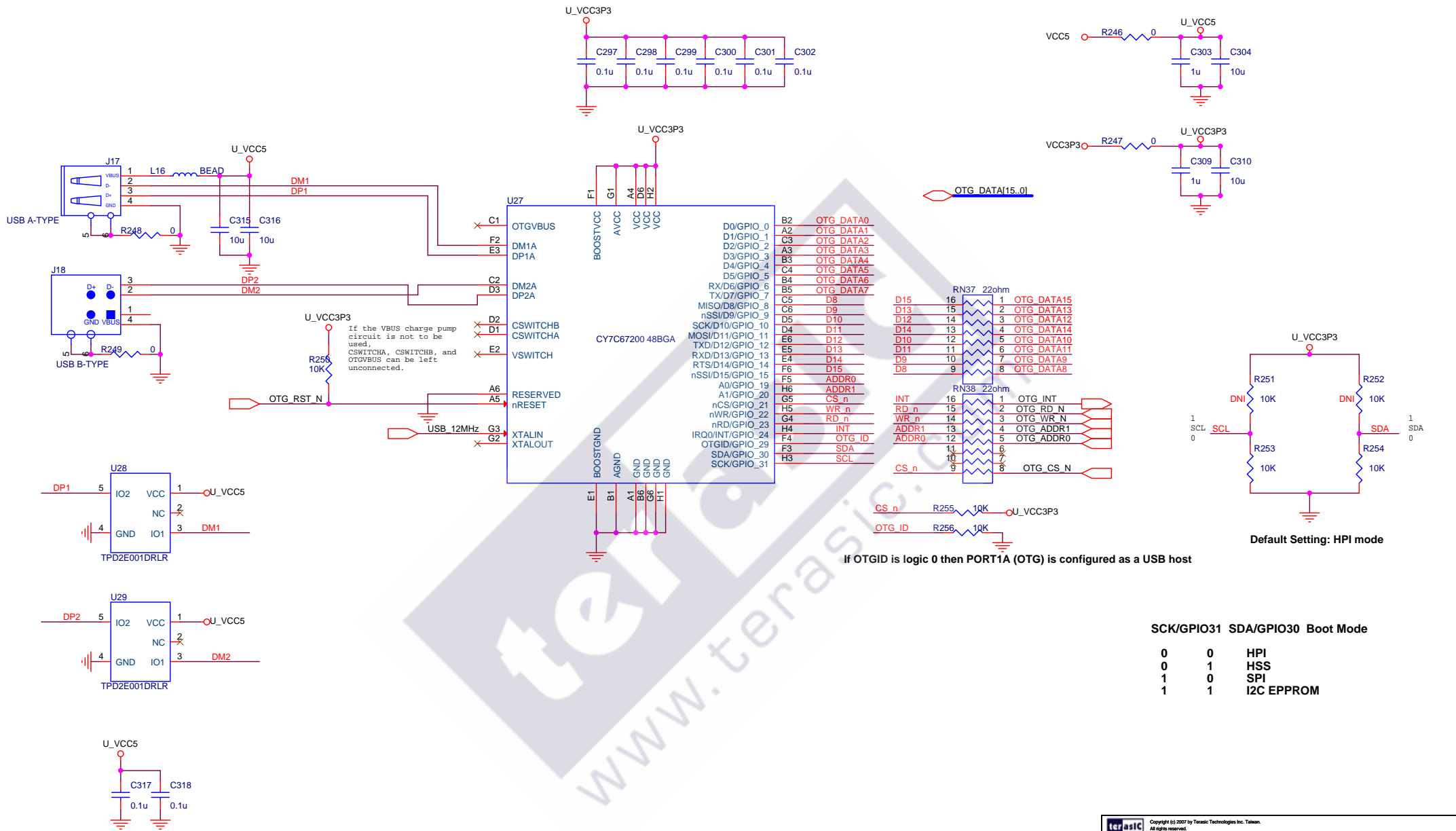
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Title

DE2-115 Main Board

Size A	Document Number WM8731 Audio	Rev D
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Date: Tuesday, April 16, 2013 **Sheet** 19 **of** 28



If OTGID is logic 0 then PORT1A (OTG) is configured as a USB host

SCK/GPIO31 SDA/GPIO30 Boot Mode

0	0	HPI
0	1	HSS
1	0	SPI
1	1	I2C EEPROM

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Title DE2-115 Main Board

Size B Document Number CY7C67200 **Rev D**

Date: Tuesday, April 16, 2013 **Sheet** 20 **of** 28

OTG_DATA[15..0]
LCD_DATA[7..0]

DRAM_DQ[31..0]
DRAM_ADDR[12..0]
DRAM_DQM[3..0]

SRAM_ADDR[19..0]
SRAM_DQ[15..0]

U12A

AUD_ADCLRCK	C2	DIFFIO_L1n/DQ2L
AUD_ADCDAT	D2	DIFFIO_L2p/DQ2L
AUD_DACDAT	D1	DIFFIO_L2n/DQ2L
PS2_CLK	G6	DIFFIO_L2n/DQ2L
PS2_CLK2	G5	DIFFIO_L3p/DQ2L/nRESET
AUD_DACLCK	E3	DIFFIO_L3n/DQ2L
OTG_DATA14	F3	DIFFIO_L4p/DQS2L/CQ3L.CDPCLK0
PS2_DAT2	F5	DIFFIO_L4n/DQ2L
OTG_DATA15	G4	DIFFIO_L5p/DQ2L
OTG_DATA12	G3	DIFFIO_L6p/DQ2L
OTG_DATA9	H4	DIFFIO_L6n
OTG_DATA8	H3	DIFFIO_L7p
AUD_XCK	E1	DIFFIO_L7n
		DIFFIO_L8n
AUD_BCLK	F2	DIFFIO_L9p/DM2L
OTG_DATA13	F1	DIFFIO_L9n/DQ0L
OTG_DATA4	J4	DIFFIO_L10p
OTG_DATA5	J3	DIFFIO_L10n/DQ0L
OTG_DATA11	G2	DIFFIO_L11p/DQ0L
OTG_DATA10	G1	DIFFIO_L11n
LCD_DATA5	K2	DIFFIO_L12p/DQS0L/CQ1L.DPCLK0
LCD_DATA4	K1	DIFFIO_L12n/DQ0L
OTG_DATA3	K3	DIFFIO_L13p
LCD_EN	L4	DIFFIO_L13n
LCD_DATA0	L3	DIFFIO_L14p
DRAM_DQ21	M4	DIFFIO_L14n
LCD_DATA6	M3	DIFFIO_L15p
OTG_DATA0	J6	DIFFIO_L15n
OTG_DATA2	J5	DIFFIO_L18p
		DIFFIO_L16n
OTG_DATA6	J7	DIFFIO_L17p
LCD_DATA3	K7	DIFFIO_L17n
DRAM_DQM2	K8	DIFFIO_L18p
DRAM_DQ17	L8	DIFFIO_L18n
DRAM_DQ23	L7	DIFFIO_L19p
LCD_BLON	L6	DIFFIO_L19n
DRAM_DQ20	N4	DIFFIO_L20p
DRAM_DQ19	N3	DIFFIO_L20n
DRAM_DQ16	M8	DIFFIO_L20p
DRAM_DQ22	M7	DIFFIO_L21p
LCD_DATA2	L2	DIFFIO_L21n
LCD_DATA1	L1	DIFFIO_L22n/DQ0L
LCD_RS	M2	DIFFIO_L23p
LCD_RW	M1	DIFFIO_L23n/DQ0L
DRAM_DQ18	P2	DIFFIO_L24p
DRAM_ADDR3	P1	DIFFIO_L24n/DQ0L

BANK1

H6 OTG_DATA7
IO_0 PS2_DAT
IO_1 N8 DRAM_DQM3
IO_2
H7 OTG_ADDR0
L5 LCD_ON
M5 LCD_DATA7

VREFB1N0
VREFB1N1
VREFB1N2

DIFFCLK_0n/CLK1 J1

U12B

DRAM_DQ27	R2	DIFFIO_L25p/DQ0L
DRAM_DQ26	R1	DIFFIO_L25n
DRAM_DQ25	R7	DIFFIO_L26p
DRAM_ADDR0	R6	DIFFIO_L26n
DRAM_DQ7	U3	DIFFIO_L27p/DM0L
DRAM_DQ30	U4	DIFFIO_L27n
DRAM_DQ28	R3	DIFFIO_L28p/DQ1L
DRAM_BA1	R4	DIFFIO_L28n/DQ1L
DRAM_CS_N	T4	DIFFIO_L29p/DQ1L
DRAM_DQ29	T3	DIFFIO_L29n
DRAM_DQ10	U2	DIFFIO_L30p
DRAM_DQ31	U1	DIFFIO_L30n/DQ1L
DRAM_DQ2	V4	DIFFIO_L31p/DQ1L
DRAM_DQ4	V3	DIFFIO_L31n
DRAM_DQ5	V2	DIFFIO_L32p/DQ1L
DRAM_DQ6	V1	DIFFIO_L32n/DQ1L
DRAM_DQ12	AB2	DIFFIO_L33p/DQS1L/CQ1L#.DPCLK1
DRAM_DQ10	AB1	DIFFIO_L33n
DRAM_DQ1	W2	DIFFIO_L34p/DQ1L
DRAM_DQ3	W1	DIFFIO_L34n/DM1L/BWS#1L
DRAM_RAS_N	U6	DIFFIO_L35p/DQ3L
DRAM_DQ24	U5	DIFFIO_L35n
DRAM_DQ8	Y4	DIFFIO_L36p/DQ3L
DRAM_DQ15	AC2	DIFFIO_L36n
DRAM_DQ13	AC1	DIFFIO_L37p/DQ3L
SRAM_ADDR13	AC3	DIFFIO_L37n/DQ3L
SRAM_ADDR11	AD3	DIFFIO_L38p/DQ3L
SRAM_DQ9	AD2	DIFFIO_L38n
SRAM_DQ8	AD1	DIFFIO_L39p/DQ3L
SRAM_ADDR14	AA4	DIFFIO_L39n
DRAM_DQ11	AA3	DIFFIO_L40p/DQ3L
		DIFFIO_L40n
SRAM_DQ10	AE2	DIFFIO_L41p/DQ3L
SRAM_DQ11	AE1	DIFFIO_L41n
DRAM_WE_N	V6	DIFFIO_L42p
DRAM_ADDR4	V5	DIFFIO_L42n
DRAM_ADDR1	V8	DIFFIO_L43p
DRAM_CAS_N	V7	DIFFIO_L43n
DRAM_DQM1	W4	DIFFIO_L44p
DRAM_DQ0	W3	DIFFIO_L44n
DRAM_ADDR9	Y6	DIFFIO_L45p
DRAM_ADDR8	Y5	DIFFIO_L45n
DRAM_ADDR5	W8	DIFFIO_L46p
DRAM_ADDR12	Y7	DIFFIO_L46n
DRAM_CKE	AA6	DIFFIO_L47p
DRAM_ADDR11	AA5	DIFFIO_L47n
SRAM_DQ12	AE3	DIFFIO_L48p/DQS3L/CQ3L#.CDPCLK1
SRAM_ADDR10	AF2	DIFFIO_L48n/DM3L/BWS#3L
SRAM_ADDR7	AC5	DIFFIO_L49p
SRAM_UB_N	AC4	DIFFIO_L49n
SRAM_ADDR4	AB6	DIFFIO_L50p
SRAM_ADDR6	AB5	DIFFIO_L50n

BANK2

R5 DRAM_ADDR10
AB3 DRAM_DQ14
W7 DRAM_ADDR6
IO_2 AA7 DRAM_ADDR7
IO_3

U7 DRAM_BA0
U8 DRAM_ADDR2

T7 SRAM_ADDR9
T8 SRAM_ADDR19
AB4 SRAM_ADDR12

VREFB2N0
VREFB2N1
VREFB2N2

DIFFCLK_1p/CLK2 Y2
DIFFCLK_1n/CLK3 Y1
CLOCK_50 FL_RY

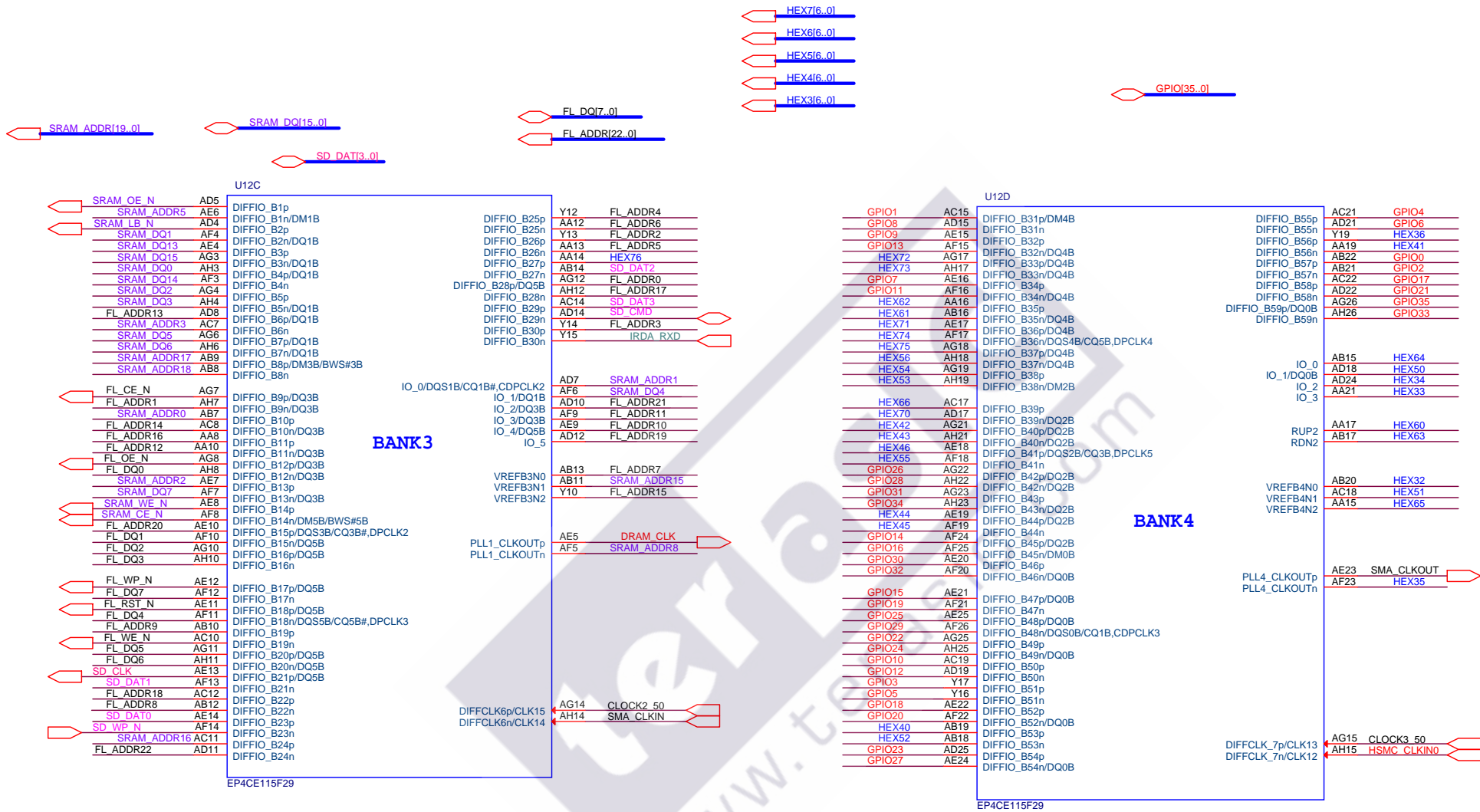
EP4CE115F29

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Title: **DE2-115 Main Board**

Size B Document Number: EP4CE115 BANK 1 and BANK 2 Rev D

Date: Tuesday, April 16, 2013 Sheet 22 of 28



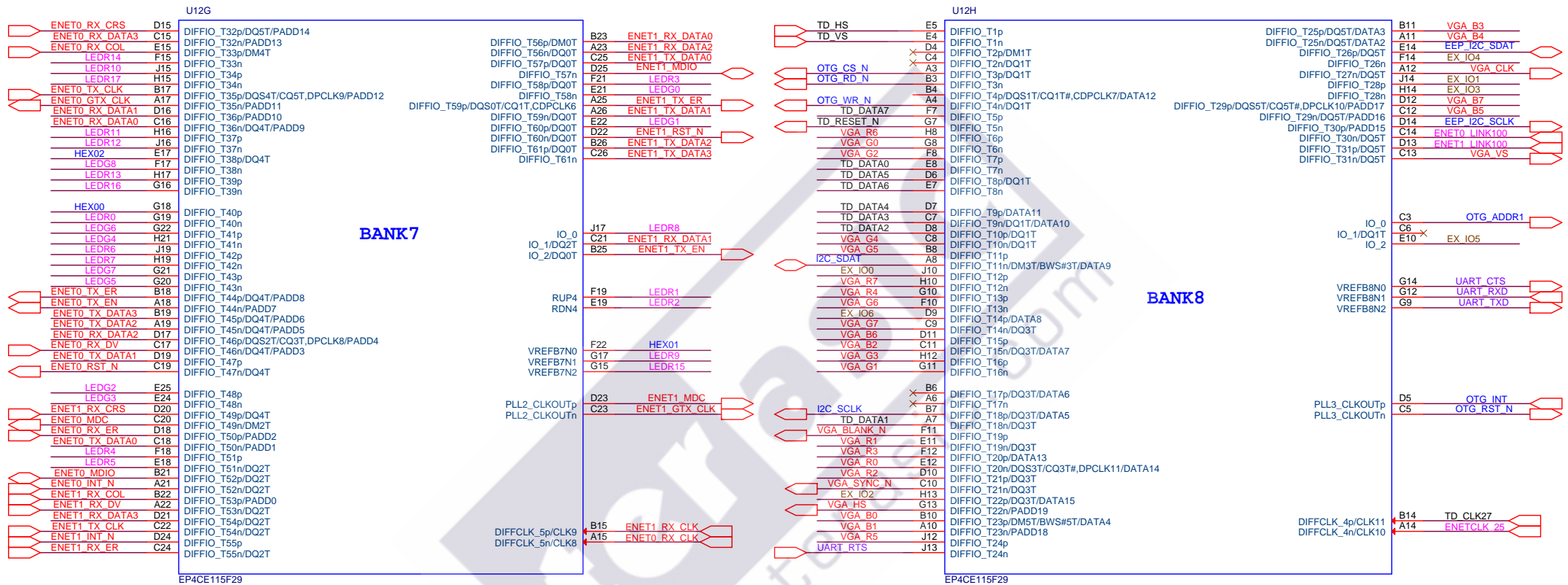
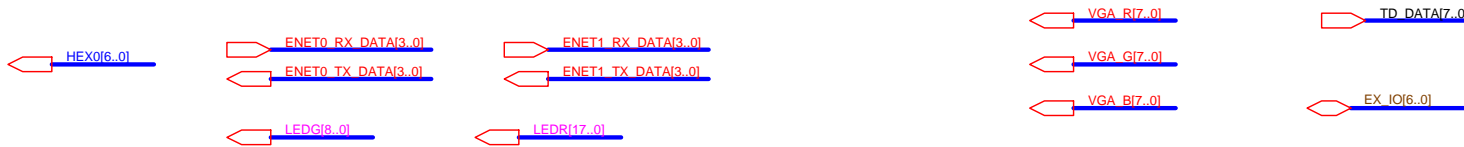
The LVDS pair can be exchanged each other, don't exchange single-ended pins with LVDS pins during PCB layout

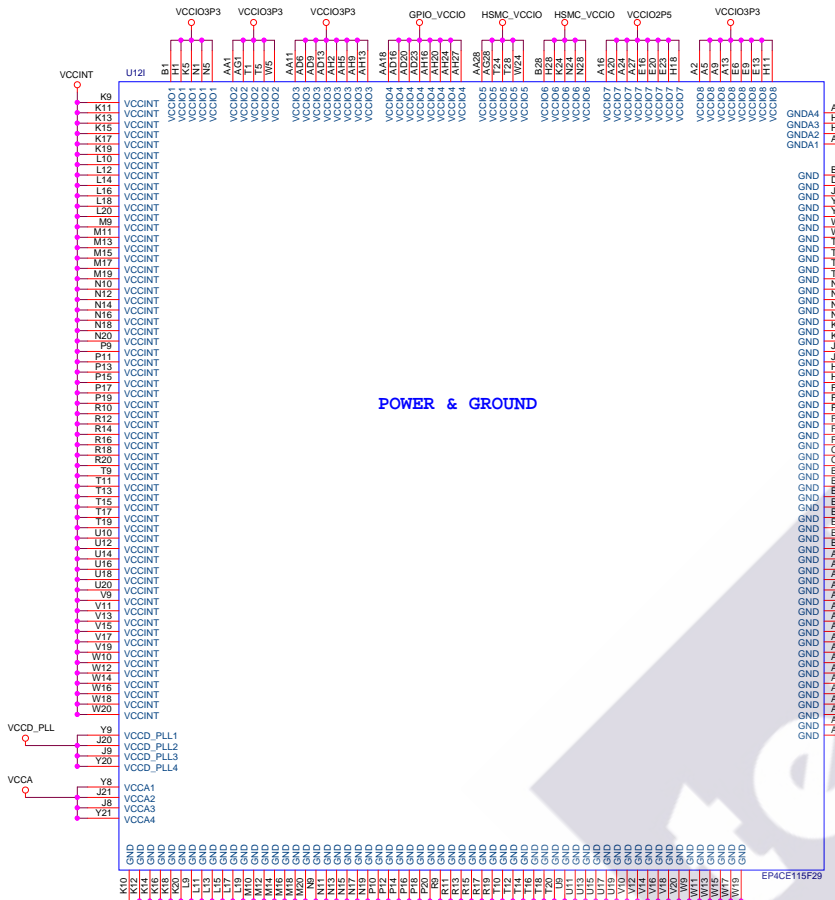
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Title: **DE2-115 Main Board**

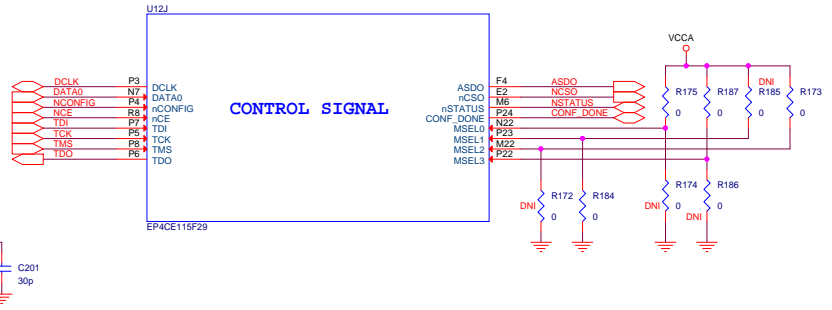
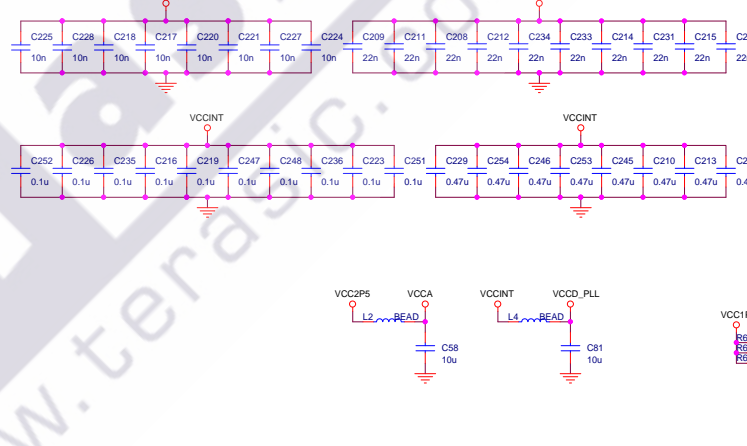
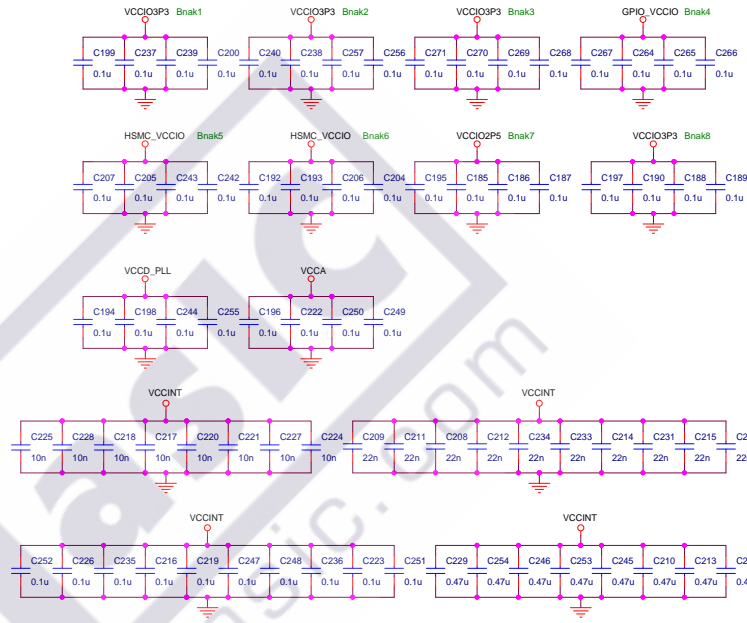
Size B Document Number: EP4CE115 BANK 3 and BANK 4 Rev D

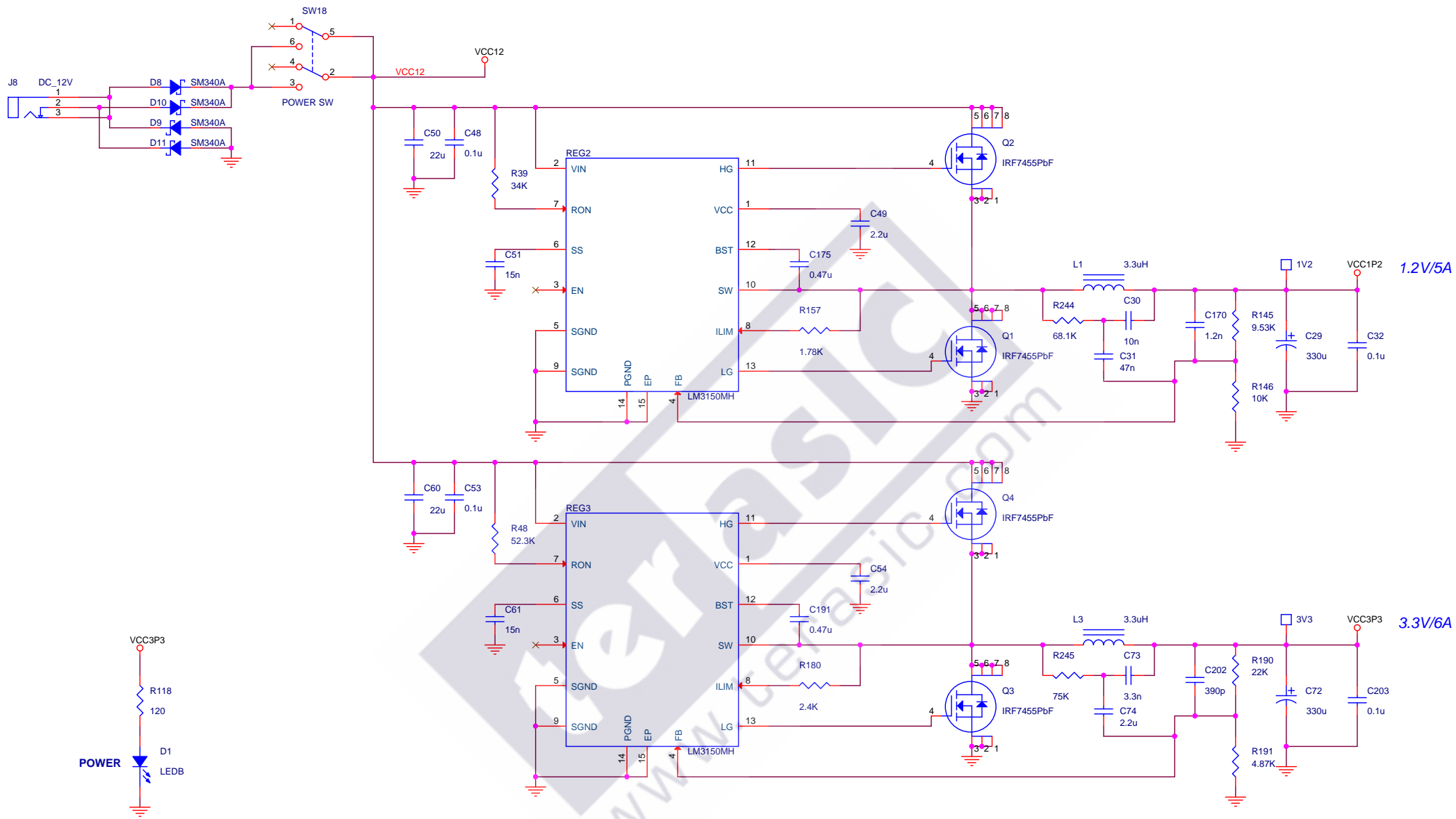
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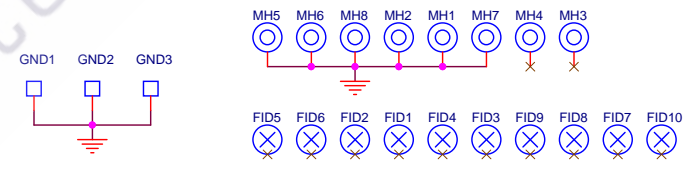
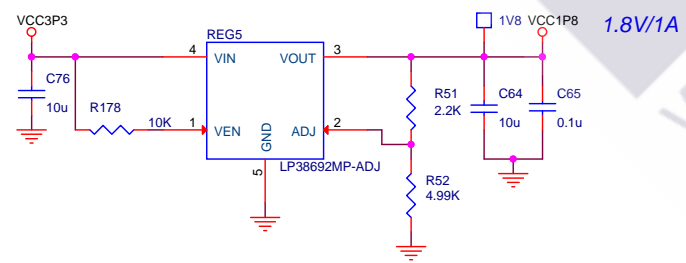
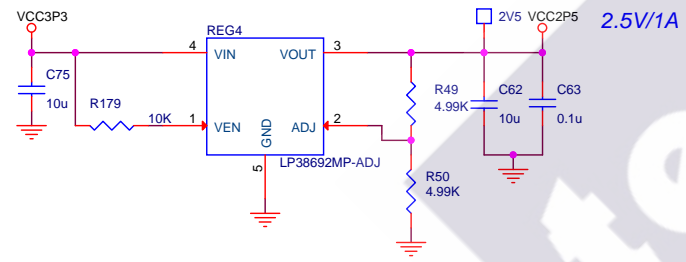
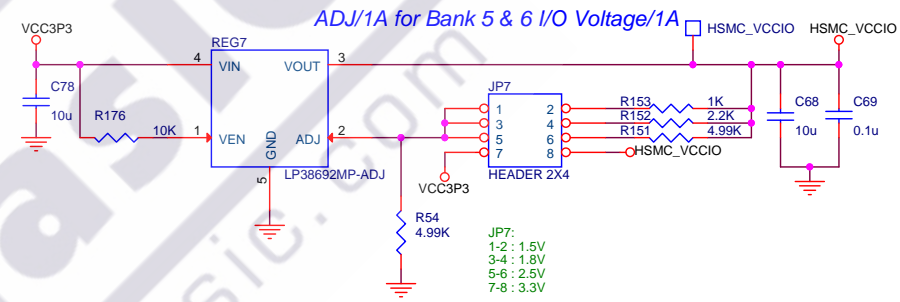
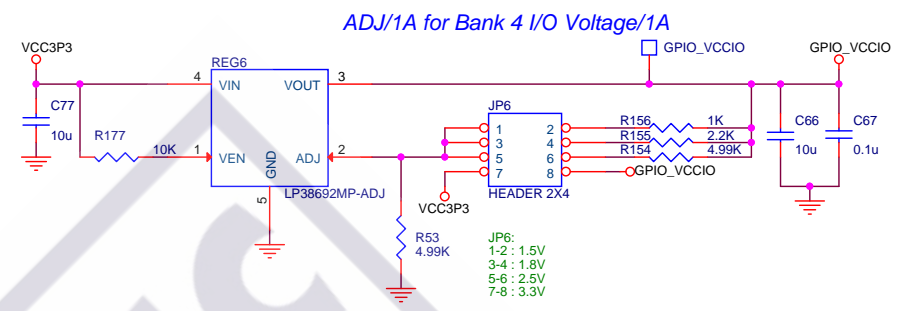
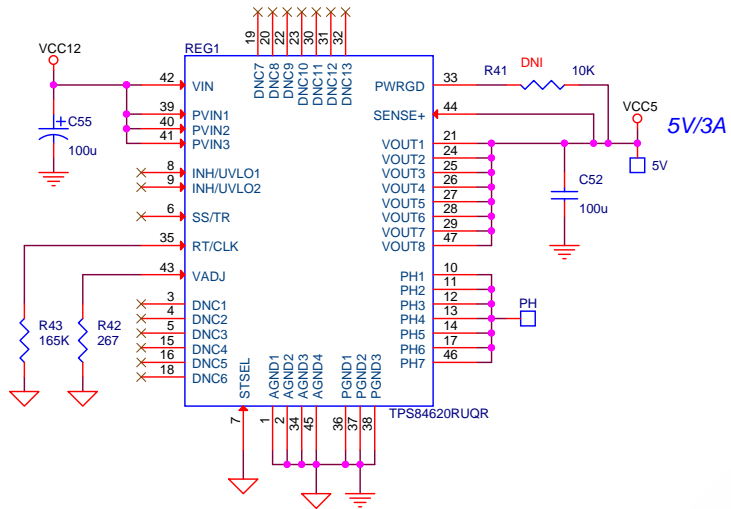


POWER & GROUND





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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	POWER 1.2V & 3.3V	D
Date:	Tuesday, April 16, 2013	Sheet 27 of 28



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Title		
DE2-115 Main Board		
Size	Document Number	Rev
B	POWER 1.8V & 2.5V & 5V	D
Date:	Wednesday, April 17, 2013	Sheet 28 of 28